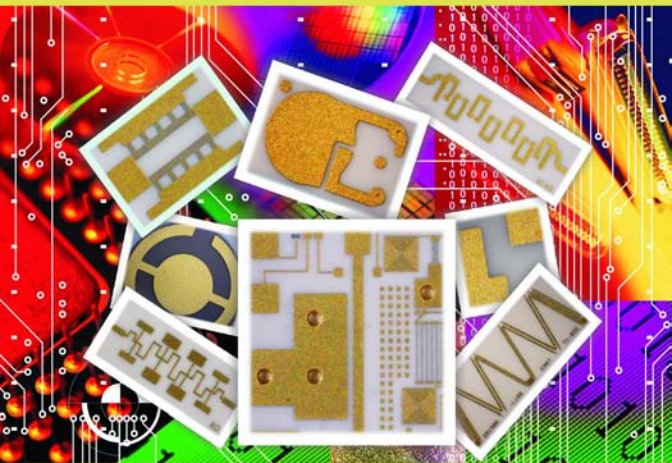




Product Guide

www.canarytec.com



广州可纳瑞电子科技有限公司
CanaryTec Co., LTD



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Company Profile

广州可纳瑞电子科技有限公司是一家集产品研发、生产、销售、技术服务为一体的高新技术企业，位于广州天河科技园；公司专注于陶瓷薄膜金属化技术及其相关产品的研发和市场化推进工作，拥有行业内一流的专业技术团队，积累了丰富的薄膜产品开发、生产及质量控制经验，相关产品已广泛应用在微波通讯、光纤通讯、LED照明等超高频、小型化、高散热要求的行业，客户主要集中在航天、军工、科研院所等单位，为扩大市场规模，公司重点发展方向已转变为民用高端光纤通讯、LED照明等行业。公司主要产品为：薄膜电阻、薄膜电容、薄膜衰减器、陶瓷垫块、陶瓷短路片、个性化薄膜电路等。



CanaryTec Co., LTD is a high-tech enterprise offering product development, manufacture, sales & technical services and located in Guangzhou Tianhe Technology Park. With more than 8 years professional working experience in Thin Film products development, manufacture, quality control, the CanaryTec specializes in Thin Film metallization (TiW, Ni, Au, TaN) on various ceramic substrates, Thin Film product development & marketing with a professional technical team. The products are been widely used in microwave communications, fiber communications, LED lighting and other application areas need super high frequency, miniaturization or high heat dissipation. Our customers are mainly concentrated in the aerospace, military, scientific research institute and the like. To enlarge our sales revenue, the CanaryTec's marketing policy has changed to civil fiber-communications, LED lighting with high-power and emerging industries. The CanaryTec will not only supply you with the highest quality Thin Film Resistors, Thin Film Capacitors, Thin Film Attenuators, Ceramic Pads (Stand Offs), Ceramic Heat Sinks & Custom Thin Film Circuits at a reasonable price, but also provide a good after-sales service.

产品测试及检验标准

Qualification Standard for Testing & Inspecting

No.	检验项目 Test Item	测试标准和条件 Standards & Condition
1	物理尺寸 Physical Dimension	Mil-STD-883G 方法2016。 Mil-STD-883G, method 2016.
2	外观 Visual Inspection	100% 外观检验, 符合或者超过Mil-STD-883G, 方法2032的要求。 100% Visual inspection to meet or exceed Mil-STD-883G, method 2032 requirements.
3	导体厚度 Conductor Thickness	导体厚度符合或者超过客户要求。 Conductor thickness to meet or exceed the customer's requirements.
4	膜层粘附性 Film Adhesion	采用ASTM B571-97胶带测试方法(3M #610 胶带)。 ASTM B571-97(Film Adhesion use 3M #610 tape).
5	膜层耐高温 High Temp. Resistance	所有薄膜产品必须在400度下维持10分钟不出现问题。 All general thin film products must be met customer requirements at 400°C for 10 Minutes.
6	键合强度 Wire Bond Strength	Mil-STD-883G, 方法2011。 Mil-STD-883G, method 2011.
7	芯片抗剪强度 Die Shear Strength	Mil-STD-883G, 方法2019。 Mil-STD-883G, method 2019.
8	金丝键合剪切强度 Wire Bond Shear Strength	EIA/JESD22-B116.
9	热冲击 Thermal Shock	Mil-Std-883G, 方法1011, 条件C。 Mil-Std-883G, method 1011 condition c.
10	客户自定义 Customization	客户可以提出自定义的产品质量检测方法。 Customer requirements of product quality testing are available.

基片及其金属化技术参数一览

Performance for Substrate & Metallization

基片材质 Substrate Material		纯度 Purity	表面粗糙度 CLA Surface Roughness	介电常数 Dielectric Constant	损耗因素 Dissipation Factor	导热率 Thermal Conductivity
编号 Code No.	品名 Description	%	μm (μinch)	@1MHz	@1MHz	W/mK
A	三氧化二铝（即烧型） Alumina (As fired)	96.0	<0.64 (25.0)	9.5	0.0003	24.7
B	三氧化二铝（即烧型） Alumina (As fired)	99.6	<0.08(3.0)	9.9	0.0001	29.3
C	三氧化二铝（抛光型） Alumina (Polished)	99.6	<0.03 (1.0)	9.9	0.0001	29.3
D	氮化铝（即烧型） Aluminum Nitrid (As fired)	99.0	<0.25 (10.0)	9.0	0.0004	170~230
E	氮化铝（抛光型） Aluminum Nitrid (Polished)	99.0	<0.05 (2.0)	9.0	0.0004	170~230
F	氧化铍（即烧型） Beryllium-Oxide(As fired)	99.5	N/A	6.5	0.0004	270
G	氧化铍（抛光型） Beryllium-Oxide(Polished)	99.5	<0.10 (4.0)	6.5	0.0004	270
H	硅 Silicon	99.99	<0.0025(0.1)	11.8	0.005	125
I	非晶态二氧化硅 Fused Silicon Quartz	99.99	<0.0025(0.1)	3.8	0.000015	1.4
J	蓝宝石 Sapphire	99.99	<0.0025(0.1)	9.3~11.4	0.00086/0.0003	40
K	钛酸盐（抛光型） Titanates (Polished)	N/A	<0.08(3.0)	38~200	0.0004	1.8~4.2
L	铁氧体（抛光） Ferrite/Garnet (Polished)	N/A	<0.40(16.0)	14.5~17.6	N/A	N/A

基片标准尺寸: 长&宽 1.5, 2.0, 3.0, 3.25, 4.0 inches; 厚度 0.010, 0.015, 0.020, 0.025, 0.040 inches.
Standard Size of Substrate: Length & Width 1.5, 2.0, 3.0, 3.25, 4.0 inches; Thickness 0.010, 0.015, 0.020, 0.025, 0.040 inches.

功能 Function	金属种类 Metal Type	典型范围 Typical Range	备注 Notes
电阻层 Resistor	氮化钽 TaN	25~100 Ohms/square	标准方阻为每方50欧姆 Standard Resistor 50 Ohms/square
粘附层 Adhesion	钛钨 TiW 氮化钽 TaN	300~800 Å 400~1500 Å	钛钨层在不含电阻的电路中起粘附层作用 TiW is the bottom adhesion layer for circuits without resistors.
阻挡层 Barrier	镍 Nickel	800~2000 Å	镍层可以改善金属层的可焊性 Ni layer can improve the metal solderability
导线层 Conductor	金 Gold	5~300 Microinches	支持细线条设计 Fine line design available

金属化结构 Metallization	典型运用 Typical Applications	安装方式 Attach Methods	注释 Comments	最高耐温 Max. Temp. °C
TIW/Au	含导体不含电阻的标准结构 Standard Thin Film metal system for conductors without resistors	金锡、金硅、金镍共晶, 导电胶 Au/Sn, Au/Si, Au/Ge-Eutectic, Epoxy	适合铝线键合和引线键合, 金厚度为 0.25~0.5 微米, 适合在 100 度以上使用, 金厚度大于 100 微米时, 适合在 100 度以上使用	450
TIW/Ni/Au	高温对可焊性有要求的器件结构 Devices processed at higher temperatures requiring a solderable film	金锡、金硅、金镍共晶, 导电胶 Au/Sn, Au/Si, Au/Ge-Eutectic, Sn/Pb, Epoxy	保持 Gold 5 到 20 微米厚 for the Lead solder, maintain Gold over 100 for wire bonding.	400
TaN/TiW/Au	标准带电阻的薄膜结构 Standard Thin Film metal for resistors	金锡、金硅、金镍共晶, 导电胶 Au/Sn, Au/Si, Au/Ge-Eutectic, Epoxy	Ta/Ni 化膜提供良好的耐湿性能 Passivated Ta/Ni films offer good humidity resistance	450
TaN/TiW/Ni/Au	高温对可焊性有要求的器件结构 Devices processed at higher temperatures requiring a solderable film	金锡、金硅、金镍共晶, 导电胶 Au/Sn, Au/Si, Au/Ge-Eutectic, Sn/Pb, Epoxy		400

薄膜电阻及网络

Thin Film Resistors & Networks

电阻材质 Resistance Material	电阻温度系数 Resistance TCR	电阻最小尺寸 Min Resistance Size	焊盘最小尺寸 Min Pad Size
氮化钽 TaN	$\pm 100 \text{ ppm/}^{\circ}\text{C}$	$0.050 \times 0.050 \text{ mm}$	$0.100 \times 0.100 \text{ mm}$

1、标准薄膜电阻

Standard Thin Film Resistors

尺寸 Size 阻值 Resistance	0201(0.51*0.25mm)		0402(1.02*0.51mm)		0603(1.52*0.76mm)	
	J ($\pm 5\%$)	K ($\pm 10\%$)	J ($\pm 5\%$)	K ($\pm 10\%$)	J ($\pm 5\%$)	K ($\pm 10\%$)
50 Ω	R0201B500J	R0201B500K	R0402B500J	R0402B500K	R0603B500J	R0603B500K
100 Ω	R0201B101J	R0201B101K	R0402B101J	R0402B101K	R0603B101J	R0603B101K
200 Ω	R0201B201J	R0201B201K	R0402B201J	R0402B201K	R0603B201J	R0603B201K



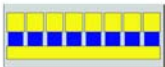
- 1、以上产品型号均对基片材质 99.6% Al_2O_3 而言。The above products code no. refers to the material of 99.6% Al_2O_3 。
2、基片标准厚度 0.010 inches (0.254mm)。Standrd Thickness 0.010 inches(0.254mm)。

2、薄膜电阻网络

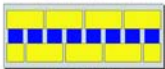
Thin Film Resistors Networks



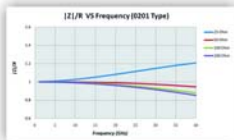
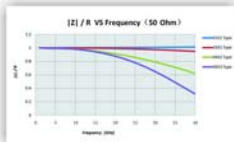
隔离型电阻网络
Isolated Connection Resistor Array



共电极型电阻网络
Common Connection Resistor Array



串联型电阻网络
Series Connection Resistor Array

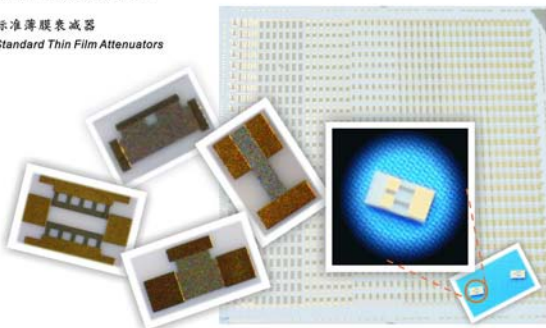


薄膜衰减器

Thin Film Attenuators

标准薄膜衰减器

Standard Thin Film Attenuators



尺寸 Size	0402(1.02*0.51mm)			0603(1.52*0.76mm)		
	D (±0.50dB @DC~18GHz)	E (±0.75dB @DC~18GHz)	G (±1.00dB @DC~18GHz)	D (±0.50dB @DC~18GHz)	E (±0.75dB @DC~18GHz)	G (±1.00dB @DC~18GHz)
1dB	A0402B010D			A0603B010D		
2dB	A0402B020D			A0603B020D		
3dB	A0402B030D			A0603B030D		
4dB	A0402B040D			A0603B040D		
6dB	A0402B060D			A0603B060D		
8dB	A0402B080D			A0603B080D		
10dB	A0402B100D			A0603B100D		
16dB		A0402B160E			A0603B160E	
32dB			A0402B320G			A0603B320G

1. 以上产品型号均指简单T型、π型衰减器而言。The above products code no. refers to the simple T & π type attenuators.
2. 以上产品型号均对基片材质 99.6% AL₂O₃而言。The above products code no. refers to the material of 99.6% AL₂O₃.
3. 基片标准厚度 0.010 inches (0.254mm)。Standrd Thickness 0.010 inches(0.254mm).
4. 回波损耗 VSWR (Max: 1) 1.35 : 1 @ DC~18GHz.

我们接受客户各种薄膜衰减器的个性化设计和制作需求。

We can design and manufacture Thin Film Attenuator to meet your individual requirements.

陶瓷垫片

Submounts

标准支撑片、热沉片、短路片

Standard Standoffs, Heat Sink & Shorter



示意图 Diagram				
代号 Code	A	B	C	D
长宽尺寸 L & W Size				
0.010"×0.010 inch (0.254"×0.254 mm)	M1010A010A	M1010A010B	M1010A010C	M1010A010D
0.015"×0.015 inch (0.381"×0.381 mm)	M1515A010A	M1515A010B	M1515A010C	M1515A010D
0.020"×0.020 inch (0.508"×0.508 mm)	M2020A010A	M2020A010B	M2020A010C	M2020A010D
0.025"×0.025 inch (0.635"×0.635 mm)	M2525A010A	M2525A010B	M2525A010C	M2525A010D
0.030"×0.030 inch (0.762"×0.762 mm)	M3030A010A	M3030A010B	M3030A010C	M3030A010D
0.035"×0.035 inch (0.889"×0.889 mm)	M3535A010A	M3535A010B	M3535A010C	M3535A010D
0.040"×0.040 inch (1.016"×1.016 mm)	M4040A010A	M4040A010B	M4040A010C	M4040A010D
0.050"×0.050 inch (1.270"×1.270 mm)	M5050A010A	M5050A010B	M5050A010C	M5050A010D



1. 以上产品型号均对基片材质 96.0% Al_2O_3 而言。The above products code no. refers to the material of 96.0% Al_2O_3 .
2. 基片标准厚度 0.010 inches (0.254mm)。Standrd Thickness 0.010 inches(0.254mm).
3. A型产品留边量为 0.002inches (0.051mm)。The border width of A type is 0.002inches (0.051mm).

客户定制产品

Customized Products

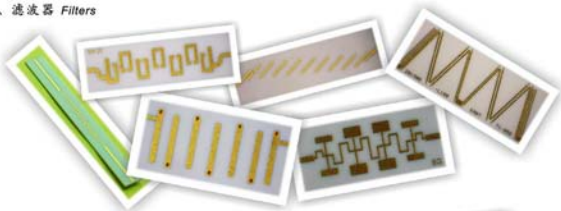


我们接受客户各种薄膜陶瓷垫块的个性化设计和制作要求。
We can design and manufacture Thin Film Submount to meet your individual requirements.

典型应用

Typical Applications

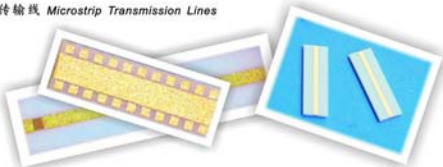
1、滤波器 Filters



2、耦合器 Couplers



3、微带传输线 Microstrip Transmission Lines



4、LED陶瓷支撑座 LED Submounts



薄膜电路设计手册

Thin Film Circuit Design Rules

1、陶瓷基片的选择 The Choice of Ceramic substrates

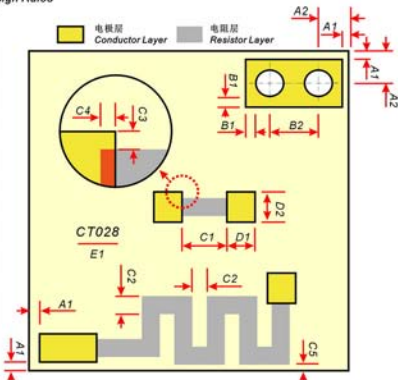
项目 Item	工作频率 Frequency	DC-6GHz	DC-18GHz	DC-40GHz	DC-60GHz
基片厚度的选择 (99.6% Al_2O_3) The choice of substrate thickness (99.6% Alumina)		0.635mm (0.025 inch)	0.381mm (0.015 inch)	0.254mm (0.010 inch)	0.127mm (0.005 inch)
基片表面粗糙度与光刻精度关系 Substrate surface roughness and lithography accuracy		0.020mm @ 烧结型 Al_2O_3 基片 Fired Alumina Substrate 0.012mm @ 抛光型 Al_2O_3 基片 Polished Alumina Substrate			

2、薄膜电路基本技术指标 The Thin Film Circuit Performances

序号 No.	项目 Item	参数 Performance
1	有效面积 Effective area	40*40mm @ 2*2 inches Substrate 60*60mm @ 3*3 inches Substrate
2	最小线宽/缝宽 Minimum Line Width / Silt Width	0.020mm
3	最小孔径 Minimum Hole Diameter	0.200mm
4	最小径厚比 Minimum Hole Diameter-Thickness Ratio	0.8

3、电路设计规则 The Circuit Design Rules

编号 Code	参数 Feature	最小值 Minimum
A1	电极留边量 Metalization Pullback	0.050 mm
A2	孔中心到边缘距离 Hole Center to Border Spacing	2R
B1	孔边缘到电极的距离 Via Hole Cover Pad	0.050 mm
B2	孔径 Pitch of Holes	4R
C1	电阻长度 Resistor Length	0.050 mm
C2	电阻宽度/间距 Resistor Width/ Gap	0.050 mm
C3	电阻对电极预留量 Conductor Margin of Resistor	0.025 mm
C4	电阻电极重叠量 Overlap	0.050 mm
C5	电阻留边量 Resistor Pullback	0.050 mm
D1	电极长度 Conductor Length	0.100 mm
D2	电极宽度 Conductor Width	0.100 mm
E1	标识位置 Mark Position	空白处 the space



4、TaN电阻设计规则 The TaN Resistors Design Rules

TaN薄膜电阻是在导体层下溅射一层氮化钽薄膜，然后通过有选择性的蚀刻电阻薄膜制成。下面的资料可以用来设计您所希望的电阻阻值以及获得其它关于Ta/N薄膜电阻的信息。

Thin film TaN resistors are fabricated by sputtering a thin film of Tantalum Nitride under the conductor layer and selectively etching the resistor elements. The following information can be used to obtain desired resistor value and other parameters.

TaN 薄膜电阻通常是按照以下经验公式设计的：

The design of thin film TaN resistor is governed by the following equation:

$$R = \rho L / (W t)$$

其中 Where: R =电阻的电阻值 Total Resistance(Ω)

ρ =电阻材料的体积电阻率 Bulk Resistivity of Resistor Material($\Omega \cdot \text{cm}$)

L =电阻薄膜的长度 Resistor Length(cm)

W =电阻薄膜的宽度 Resistor Width(cm)

t =电阻薄膜的厚度 Resistor Thickness(cm)

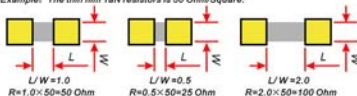
为设计方便，假设 $L=W$ 时，方块电阻 $R_{\text{square}} = R_s = \rho/t$ (Ω/Square)，那么，电阻阻值 $R = R_{\text{square}} \times (L/W)$ 。

To ease design, assumes $L=W$, $R_{\text{square}} = R_s = \rho/t$ (Ω/Square), so that $R = R_s \times (L/W)$.

假设：以下Ta/N薄膜电阻设计时，采用的方块为50欧姆/方。

Example: The thin film TaN resistors is 50 Ohm/Square.

项目 Item	参数 Performance
方块电阻值 Square Resistance	50 Ω/Square (20~200 Ω)
-55~+125℃电阻温度变化系数 TCR (-55~+125℃)	$\pm 100 \text{ ppm}$
1000小时+125℃阻值稳定性 Stability (1000 Hr+125℃)	0.02 %
短时耐时高温 (5分钟) Short Term Max E7(5minutes)	450℃
最小电阻误差 Minimum Resistor Tolerance	$\pm 5.0 \%$
25℃时额定最大承受电流 (mA/mm) Maximum Rated Current(mA/mm)@25℃	0.12



5、对技术文件的基本要求 The requirements of technical documents

序号 No.	项目 Item	要求 Requirements
1	文件格式 File Format	必须采用CAD文件，可以接受 DXF或 DWG后级的文件。 Must be in AutoCAD DXF or DWG file.
2	图形比例 Drawing scale	1 : 1
3	图形单位 Drawing unit	毫米 mm
4	图层及线条颜色标识 Layer&Line colour Identification	图例1 Layer 1 图例2 Layer 2 图例3 Layer 3 图例4 Layer 4 图例5 Layer 5 图例6 Layer 6 产品轮廓线 Product Outline 导体轮廓线 Conductor Outline 电阻轮廓线 Resistors Outline 孔轮廓线 Holes Outline 外框及标注颜色 Frame&Mark Line colour 客户自定义 Customization
5	图形及线条 Drawing & Line	(1) 所有图形必须是封闭的。 Zero width polylines are needed to create closed boundary polygons for all geometries. (2) 避免图形重叠和不必要的线条。 Avoid double entities or extraneous lines. (3) 图形不需要颜色填充。 All geometries only need their frame, not need fill in. 正确图形 Acceptable 错误图形 Unacceptable 错误图形 Unacceptable

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